

REMARKS

Claims 2-34 were canceled without prejudice. Claim 1 was amended. Claims 35-53 were added. Examination of the claims on the merits is respectfully requested.

Independent claims 1 and 49 recite that the opening through the multi-layer dielectric structure, which is formed partially by an isotropic etch (with a nitride etch stop layer within the dielectric structure) and partially by an anisotropic etch, is etched through the patterned resist layer without stripping the resist between etch steps. JP '958, cited in the parent application, teaches removal of photoresist 112 after wet (isotropic) etching and before dry (anisotropic) etching. See July 2000 translation of JP '958 by Diplomatic Language Services, Inc., page 7, lines 13-16. Instead, JP '958 teaches reliance upon the thickness of the upper (oxide) portion of the dielectric structure during completion of the contact opening by dry etching. Accordingly, JP '958 does not teach or suggest the present invention.

Independent claim 42 recites a complete opening through the multi-layer dielectric structure with the patterned resist layer in place. As noted above, JP '958 teaches removing the photoresist layer before completing the contact opening by anisotropic etch. The structure recited is not shown or suggested by JP '958.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 was amended herein as follows:

1. (amended) A fabrication method, comprising the steps of:

[(a) providing an integrated circuit structure which has been fabricated through the formation of transistors;]

[(b)]forming [an interlevel]a dielectric structure over [said transistors]a contact region, [said interlevel]the dielectric [including at least]structure comprising:

[(i)]a [lower]first layer [having]formed from a first [composition comprising a silicate glass doped with a gettering agent,]material; and

[(ii)]a [middle]second layer [having]overlying the first layer and formed from a second [composition which is different from said first composition, and]material which may be selectively etched with respect to the first material;

[(iii) an upper layer having a third composition which is different from said second composition;]

forming and patterning a resist layer over the dielectric structure;

[(c)]selectively etching [through said upper]the second layer[, using an essentially isotropic] through an opening through the patterned resist layer utilizing an etch [process] which is selective [to said]of the first material over the second [composition]material; and

[(d)]without stripping the resist layer, etching [through said middle and lower layers,

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18 using an essentially anisotropic etch process, to expose portions of said transistors; and
19 (e) depositing and patterning a thin-film conductor layer, to interconnect said
20 transistors]the dielectric structure through the opening within the patterned resist layer and any
21 etched region within the second layer to form a contact opening extending through the dielectric
22 structure and exposing the contact region.

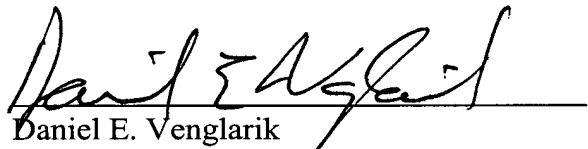
If any issue arises, or if the Examiner has any suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@novakov.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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